

data frame;

providing permitted address information;

providing an IDLE character generator;

determining if said incoming data frame is addressed to an unconfigured source address / destination address pair;

operative if said incoming data frame is not addressed to an unconfigured source address / destination address pair, allowing said data frame to pass to the destination address; and

operative if said incoming data frame is addressed to an unconfigured source/destination addressed pair, replacing said incoming data frame with IDLE characters.

12. The method of claim 11, wherein said incoming data frame comprises a request to access information, further comprising the step of disallowing access by said incoming data frame to said requested information.

13. The method of claim 11, further comprising the steps of:

receiving serial data comprising said data frame;

converting said serial data to parallel data, wherein said parallel data comprises said source address and said destination address;

comparing said parallel data to said permitted address information;

operative if said incoming data frame is not addressed to an unconfigured source/destination addressed pair, converting said parallel data to said serial data.

14. The method of claim 13, further comprising the steps of:

placing said parallel data into a regulator;

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providing a trigger circuit, wherein said trigger circuit is in communication with said regulator;

operative if said incoming data frame is not addressed to an unconfigured source/destination addressed pair, triggering said regulator to pass said parallel data to said encoder.

15. The method of claim 14, further comprising the steps of:

providing a deserializer,

providing a decoder;

providing said serial data to said deserializer;

converting said serial data to a plurality of ten bit parallel words;

directing said plurality of parallel words to said decoder;

packaging said plurality of words in groups of four as 32-bit words comprising a parity bit for each byte.

16. The method of claim 15, further comprising the steps of:

providing said 32-bit words to a data first in/first out block;

locating the 32-bit word comprising said source address; and

locating the 32-bit word comprising said destination address.

17. The method of claim 16, further comprising the steps of:

comparing said source address to said permitted address information;

operative if said source address matches said permitted address information, comparing said destination address to said permitted address information; and

operative if said destination address matches said permitted address information,

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passing said frame data through said data first in/first out block.

18. The method of claim 17, further comprising the steps of:

detecting a start of frame signal;

operative if said source address does not match said permitted address information,

replacing each of said 32-bit words with IDLE characters; and

detecting an end of frame signal.

19. The method of claim 17, further comprising the steps of:

detecting a start of frame signal;

operative if said destination address does not match said permitted address information,

replacing each of said 32-bit words with IDLE characters; and

detecting an end of frame signal.

20. A method to limit access to information using a fibre channel arbitrated loop system, comprising the steps of:

receiving an incoming data frame, wherein said data frame comprises serial data;

providing a deserializer,

providing said serial data to said deserializer;

converting said serial data to a plurality of ten bit parallel words;

providing a regulator;

providing said plurality of parallel words to said regulator;

providing a trigger circuit, wherein said trigger circuit is in communication with said regulator;

providing a decoder;

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providing said plurality of parallel words to said decoder;

packaging said plurality of parallel words in groups of four as 32-bit words comprising a parity bit for each byte;

providing a data first in/first out block;

providing said 32-bit words to a data first in/first out block;

detecting a start of frame signal;

locating the 32-bit word comprising said source address;

locating the 32-bit word comprising said destination address.

providing permitted address information;

providing an encoder;

providing an IDLE character generator;

comparing said source address to said permitted address information;

operative if said source address does not match said permitted address information,

replacing each of said 32-bit words with IDLE characters;

operative if said source address matches said permitted address information, comparing said destination address to said permitted address information;

operative if said destination address does not match said permitted address information,

replacing each of said 32-bit words with IDLE characters;

operative if said destination address matches said permitted address information:

triggering said regulator to pass said parallel data to said encoder;

converting said plurality of parallel words to said serial data; and

passing said serial data to said destination location.

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21. An article of manufacture for use in a fibre channel configuration network system comprising a computer useable medium having computer readable program code disposed therein for limiting access to information, the computer readable program code comprising a series of computer readable program steps to effect:

inspecting an incoming data frame;

determining the source address and the destination addresses included in said incoming data frame;

determining if said incoming data frame is addressed to an unconfigured source address / destination address pair;

operative if said incoming data frame is not addressed to an unconfigured source address / destination address pair, allowing said data frame to pass to the destination address; and

operative if said incoming data frame is addressed to an unconfigured source/destination addressed pair, replacing said incoming data frame with IDLE characters.

22. The article of manufacture of claim 21, wherein said incoming data frame comprises a request to access information, wherein said computer readable program code further comprises a series of computer readable program steps to effect disallowing access by said incoming data frame to said requested information.

23. The article of manufacture of claim 21, wherein said computer readable program code further comprises a series of computer readable program steps to effect:

receiving serial data comprising said data frame;

converting said serial data to parallel data, wherein said parallel data comprises said

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source address and said destination address;

comparing said parallel data to previously-determined permitted address information;

operative if said incoming data frame is not addressed to an unconfigured

source/destination addressed pair, converting said parallel data to said serial data.

24. The article of manufacture of claim 23, wherein said computer readable program code further comprises a series of computer readable program steps to effect:

placing said parallel data into a regulator in communication with a triggering circuit and an encoder;

operative if said incoming data frame is not addressed to an unconfigured

source/destination addressed pair, triggering said regulator to pass said parallel data to said encoder.

25. The article of manufacture of claim 24, wherein said computer readable program code further comprises a series of computer readable program steps to effect:

providing said serial data to said deserializer in communication with a decoder;

converting said serial data to a plurality of ten bit parallel words;

directing said plurality of parallel words to said decoder; and

packaging said plurality of parallel words in groups of four as 32-bit words comprising a parity bit for each byte.

26. The article of manufacture of claim 25, wherein said computer readable program code further comprises a series of computer readable program steps to effect:

providing said 32-bit words to a data first in/first out block;

locating the 32-bit word comprising said source address; and

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locating the 32-bit word comprising said destination address.

27. The article of manufacture of claim 26, wherein said computer readable program code further comprises a series of computer readable program steps to effect:

comparing said source address to said permitted address information;

operative if said source address matches said permitted address information, comparing said destination address to said permitted address information; and

operative if said destination address matches said permitted address information, passing said frame data through said data first in/first out block.

28. The article of manufacture of claim 27, wherein said computer readable program code further comprises a series of computer readable program steps to effect:

detecting a start of frame signal;

operative if said source address does not match said permitted address information, replacing each of said 32-bit words with IDLE characters; and

detecting an end of frame signal.

29. The article of manufacture of claim 27, wherein said computer readable program code further comprises a series of computer readable program steps to effect:

detecting a start of frame signal;

operative if said destination address does not match said permitted address information, replacing each of said 32-bit words with IDLE characters; and

detecting an end of frame signal.

30. An article of manufacture for use in a fibre channel configuration network system comprising a computer useable medium having computer readable program code

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disposed therein for limiting access to information using a fibre channel protocol, the computer readable program code comprising a series of computer readable program steps to effect:

receiving an incoming data frame, wherein said data frame comprises serial data;

providing said serial data to a deserializer in communication with a decoder;

converting said serial data to a plurality of ten bit parallel words;

providing said plurality of parallel words to a regulator in communication with a triggering circuit and an encoder;

providing said plurality of parallel words to said decoder;

packaging said plurality of parallel words in groups of four as 32-bit words comprising a parity bit for each byte;

providing said 32-bit words to a data first in/first out block;

detecting a start of frame signal;

locating the 32-bit word comprising said source address;

locating the 32-bit word comprising said destination address.

comparing said source address to said permitted address information;

operative if said source address does not match said permitted address information, replacing each of said 32-bit words with IDLE characters;

operative if said source address matches said permitted address information, comparing said destination address to said permitted address information;

operative if said destination address does not match said permitted address information, replacing each of said 32-bit words with IDLE characters;

operative if said destination address matches said permitted address information:

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triggering said regulator to pass said parallel data to said encoder;
converting said plurality of parallel words to said serial data; and
passing said serial data to said destination location.

31. A computer program product usable with a programmable computer processor having computer readable program code embodied therein to limit access to information using a fibre channel protocol, comprising:

computer readable program code which causes said programmable computer processor to inspect an incoming data frame;

computer readable program code which causes said programmable computer processor to determine the source address and the destination address included in said incoming data frame;

computer readable program code which causes said programmable computer processor to determine if said incoming data frame is addressed to an unconfigured source address / destination address pair;

computer readable program code which, if said incoming data frame is not addressed to an unconfigured source address / destination address pair, causes said programmable computer processor to pass said data frame to the destination address; and

computer readable program code which, if said incoming data frame is addressed to an unconfigured source/destination addressed pair, causes said programmable computer processor to replace said incoming data frame with IDLE characters.

32. The computer program product of claim 31, further comprising:

computer readable program code which causes said programmable computer processor

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to receive serial data comprising said data frame;

computer readable program code which causes said programmable computer processor to convert said serial data to parallel data, wherein said parallel data comprises said source address and said destination address;

computer readable program code which causes said programmable computer processor to compare said parallel data to previously-determined permitted address information;

computer readable program code which, if said incoming data frame is not addressed to an unconfigured source/destination addressed pair, causes said programmable computer processor to convert said parallel data to said serial data.

33. The computer program product of claim 32, further comprising:

computer readable program code which causes said programmable computer processor to place said parallel data into a regulator in communication with a triggering circuit and an encoder;

computer readable program code which, if said incoming data frame is not addressed to an unconfigured source/destination addressed pair, causes said programmable computer processor to trigger said regulator to pass said parallel data to said encoder.

34. The computer program product of claim 33, further comprising:

computer readable program code which causes said programmable computer processor to convert said serial data to a plurality of ten bit parallel words;

computer readable program code which causes said programmable computer processor to package said plurality of ten bit parallel words in groups of four as 32-bit words comprising a parity bit for each byte.

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35. The computer program product of claim 34, further comprising:

computer readable program code which causes said programmable computer processor to provide said 32-bit words to a data first in/first out block;

computer readable program code which causes said programmable computer processor to locate the 32-bit word comprising said source address; and

computer readable program code which causes said programmable computer processor to locate the 32-bit word comprising said destination address.

36. The computer program product of claim 35, further comprising:

computer readable program code which causes said programmable computer processor to compare said source address to said permitted address information;

computer readable program code which, if said source address matches said permitted address information, causes said programmable computer processor to compare said destination address to said permitted address information; and

computer readable program code which, if said destination address matches said permitted address information, causes said programmable computer processor to pass said frame data through said data first in/first out block.

37. The computer program product of claim 36, further comprising:

computer readable program code which causes said programmable computer processor to detect a start of frame signal;

computer readable program code which, if said source address does not match said permitted address information, causes said programmable computer processor to replace each of said 32-bit words with IDLE characters; and

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computer readable program code which causes said programmable computer processor to detect an end of frame signal.

38. The computer program product of claim 36, further comprising:

computer readable program code which causes said programmable computer processor to detect a start of frame signal;

computer readable program code which, if said destination address does not match said permitted address information, causes said programmable computer processor to replace each of said 32-bit words with IDLE characters; and

computer readable program code which causes said programmable computer processor to detect an end of frame signal.

39. A computer program product usable with a programmable computer processor having computer readable program code embodied therein to limit access to information using a fibre channel protocol, comprising:

computer readable program code which causes said programmable computer processor to receive an incoming data frame, wherein said data frame comprises serial data;

computer readable program code which causes said programmable computer processor to convert said serial data to a plurality of ten bit parallel words;

computer readable program code which causes said programmable computer processor to package said plurality of parallel words in groups of four as 32-bit words comprising a parity bit for each byte;

computer readable program code which causes said programmable computer processor to detect a start of frame signal;

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computer readable program code which causes said programmable computer processor to locate the 32-bit word comprising said source address;

computer readable program code which causes said programmable computer processor to locate the 32-bit word comprising said destination address.

computer readable program code which causes said programmable computer processor to compare said source address to previously-determined permitted address information;

computer readable program code which, if said source address does not match said permitted address information, causes said programmable computer processor to replace each of said 32-bit words with IDLE characters;

computer readable program code which, if said source address matches said permitted address information, causes said programmable computer processor to compare said destination address to said permitted address information;

computer readable program code which, if said destination address does not match said permitted address information, causes said programmable computer processor to replace each of said 32-bit words with IDLE characters;

computer readable program code which, if said destination address matches said permitted address information causes said programmable computer processor to convert said plurality of parallel words to said serial data, and to pass said serial data to said destination location.

40. A blocking apparatus to limit access to information in a fibre channel arbitrated loop system, comprising:

a decoder, wherein said decoder is capable of communication with one or more

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communication networks;

permitted address information;

a comparator, wherein said comparator is capable of communication with said decoder and with said permitted address information;

an IDLE character generator, wherein said IDLE character generator is capable of communication with said comparator;

a trigger circuit, wherein said trigger circuit is capable of communication with said comparator;

a regulator, wherein said regulator is capable of communication with said decoder and with said trigger circuit;

an encoder, wherein said encoder is in communication with said regulator.

41. The apparatus of claim 40, further comprising:

a deserializer, wherein said deserializer is capable of communication with said decoder;

a data first in / first out block, wherein said data first in / first out block is capable of communication with said decoder and with said comparator;

a multiplexor, wherein said multiplexor is capable of communication with said comparator, with said IDLE character generator, and with said data first in / first out block.

42. The apparatus of claim 41, further comprising a serializer, wherein said serializer is capable of communication with said encoder.

43. A fibre channel arbitrated loop system, comprising:

one or more information storage devices;

a hub;

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a blocking apparatus for limiting access to said one or more storage devices, wherein said blocking apparatus is capable of communication with said hub and is capable of communication with each of said one or more information storage devices, and wherein said blocking apparatus comprises:

a decoder, wherein said decoder is capable of communication with said hub;

permitted address information;

a comparator, wherein said comparator is capable of communication with said decoder and with said permitted address information;

an IDLE character generator, wherein said IDLE character generator is capable of communication with said comparator;

a trigger circuit, wherein said trigger circuit is capable of communication with said comparator;

a regulator, wherein said regulator is capable of communication with said decoder and with said trigger circuit;

an encoder, wherein said encoder is in communication with said one or more information storage devices.

44. The fibre channel arbitrated loop system of claim 43, wherein said blocking apparatus further comprises:

a deserializer, wherein said deserializer is capable of communication with said decoder;

a data first in / first out block, wherein said data first in / first out block is capable of communication with said decoder and with said comparator;

a multiplexor, wherein said multiplexor is capable of communication with said

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comparator, with said IDLE character generator, and with said data first in / first out block.

45. The fibre channel arbitrated loop system of claim 44, wherein said blocking apparatus further comprises a serializer, wherein said serializer is capable of communication with said encoder and with said one or more information storage devices.

46. A fibre channel arbitrated loop system, comprising:

a fabric switch system;

a hub;

one or more information storage devices, wherein said one or more information storage devices are capable of communication with said hub;

a blocking apparatus for limiting access to said one or more storage devices, wherein said blocking apparatus is capable of communication with said hub and is capable of communication with said fabric switch system, and wherein said blocking apparatus comprises:

a decoder, wherein said decoder is capable of communication with said hub;

permitted address information;

a comparator, wherein said comparator is capable of communication with said decoder and with said permitted address information;

an IDLE character generator, wherein said IDLE character generator is capable of communication with said comparator;

a trigger circuit, wherein said trigger circuit is capable of communication with said comparator;

a regulator, wherein said regulator is capable of communication with said decoder and with said trigger circuit;

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